Abstract of the Disclosure

A low power audio processor is disclosed which includes a bit stream processing unit for performing bit processing for an applied audio stream and for decoding the bit processed audio stream to have a format conducive to digital signal processing; a digital signal processing unit for receiving the decoded data from the bit stream processing unit to perform digital signal processing; a post processing unit for post processing audio data from the digital signal processing unit to output final audio data; and a host interface unit for interfacing with an external device to provide an audio parallel stream from the external device to the bit stream processing unit. The audio signal processor also includes a power control unit for determining the idle state for each of the bit stream processing unit, the digital signal processing unit and the post processing unit in response to: (a) a request signal and an acknowledge signal between the digital signal processing unit and the post processing unit, (b) a power down signal, and (c) a source clock to output the determined power state as a power mode signal; and an internal clock signal generator for generating clock signals, in response to the power mode signal and for outputting the clock signals to respective one of the bit stream processor, the digital signal processor and the post processor.